Listing of Claims

1. (Previously Presented) A method of forming a capacitor on an integrated circuit comprising:

forming a lower electrode on an integrated circuit substrate;

forming a nitride protection layer on the lower electrode at a first temperature without a phase change of the lower electrode and without an increase of a resistance of the lower electrode;

forming a dielectric layer on the nitride protection layer at a second temperature substantially the same as the first temperature, wherein the nitride protection layer is configured to prevent an oxidation of the lower electrode in a formation of the dielectric layer; and

forming an upper electrode on the dielectric layer.

2. (Previously Presented) The method of Claim 1, wherein the lower electrode comprises an amorphous silicon layer, a polycrystalline silicon layer and/or a composite layer thereof.

3. (Previously Presented) The method of Claim 1, wherein the nitride protection layer comprises a silicon nitride layer.

4. (Previously Presented) The method of Claim 3, wherein forming the nitride protection layer is performed at the first temperature below about 600°C using a plasma nitration process.

5. (Previously Presented) The method of Claim 3, wherein forming the nitride protection layer is performed at the first temperature below about 600°C using a chemical vapor deposition process or an atomic layer deposition process.

6. (Previously Presented) The method of Claim 3, wherein forming the nitride

protection layer is performed at the first temperature below about 600°C using a microwave-type deposition process.

7. (Previously Presented) The method of Claim 1, wherein the dielectric layer comprises a metal oxide layer.

8. (Previously Presented) The method of Claim 7, wherein the metal oxide layer comprises a TiO_2 layer, an Al_2O_3 layer, an Y_2O_3 layer, a ZrO_2 layer, an HfO_2 layer, a $BaTiO_3$ layer, an $SrTiO_3$ layer and/or a composite layer thereof.

9. (Previously Presented) The method of Claim 7, wherein forming the dielectric layer is performed at the second temperature below about 600°C using a chemical vapor deposition process or an atomic layer deposition process.

10. (Canceled).

11. (Previously Presented) The method of Claim 1, wherein the upper electrode comprises an amorphous silicon layer, a polycrystalline silicon layer, an Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and/or a composite layer thereof.

12. (Previously Presented) The method of Claim 1, wherein forming the lower electrode comprises:

forming a lower structure on the integrated circuit substrate;

forming an insulation layer pattern having a contact hole on the lower structure;

forming a conductive plug in the contact hole;

forming an oxide layer patterned to have a cylindrical shape on the insulation layer pattern and the conductive plug;

forming a conductive layer for the lower electrode on the oxide layer; and

removing the oxide layer to form the lower electrode having a cylindrical shape.

13. (Previously Presented) The method of Claim 12, wherein the nitride protection layer is directly formed on the conductive layer.

14. (Previously Presented) A method of forming a capacitor comprising:

forming a first conductive layer on a substrate;

forming a reaction-preventing nitride layer on the first conductive layer at a first temperature without a phase change of the first conductive layer and without an increase of a resistance of the first conductive layer;

forming a dielectric layer on the reaction-preventing nitride layer at a second temperature substantially the same as the first temperature, wherein the reaction-preventing nitride layer prevents an oxidation of the first conductive layer in a formation of the dielectric layer; and

forming a second conductive layer on the dielectric layer.

15. (Previously Presented) The method of Claim 14, wherein the first conductive layer comprises an amorphous silicon layer, a polycrystalline silicon layer and/or a composite layer thereof.

16. (Previously Presented) The method of Claim 14, wherein the reaction-preventing nitride layer comprises a silicon nitride layer.

17. (Previously Presented) The method of Claim 16, wherein the reaction-preventing nitride layer is formed by a plasma nitration process at the first temperature below about 600°C.

18. (Previously Presented) The method of Claim 16, wherein the reaction-preventing nitride layer is formed by a chemical vapor deposition process at the first temperature below about 600°C or by an atomic layer deposition process at the first

temperature below about 600°C.

19. (Previously Presented) The method of Claim 16, wherein the reaction-preventing nitride layer is formed by a microwave-type deposition process at the first temperature below about 600°C.

20. (Previously Presented) The method of Claim 14, wherein the dielectric layer comprises a metal oxide layer.

21. (Previously Presented) The method of Claim 20, wherein the metal oxide layer comprises at least one selected from the group consisting of a TiO_2 layer, an Al_2O_3 layer, an Y_2O_3 layer, a ZrO_2 layer, an HfO_2 layer, a $BaTiO_3$ layer, an $SrTiO_3$ layer and a composite layer thereof.

22. (Previously Presented) The method of Claim 20, wherein the dielectric layer is formed by a chemical vapor deposition process at the second temperature below about 600°C or by an atomic layer deposition process at the second temperature below about 600°C.

23. (Previously Presented) The method of Claim 14, wherein the second conductive layer comprises an amorphous silicon layer, a polycrystalline silicon layer, a Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and/or a composite layer thereof.

24. (Previously Presented) A method of forming a capacitor comprising:

forming an insulation layer pattern having a contact hole on a substrate having a lower structure;

forming a first conductive layer continuously on a sidewall portion and a bottom portion of the contact hole and on a surface portion of the insulation layer pattern;

removing the first conductive layer formed on the surface of the insulation layer

pattern;

removing the insulation layer pattern to allow the first conductive layer to remain on the sidewall portion and the bottom portion of the contact hole to form a cylindrical lower electrode;

forming a reaction-preventing nitride layer on the cylindrical lower electrode at a first temperature without a phase change of the cylindrical lower electrode and without an increase of a resistance of the cylindrical lower electrode;

forming a dielectric layer on the reaction preventing nitride layer at a second temperature substantially the same as the first temperature, wherein the reaction-preventing nitride layer prevents an oxidation of the cylindrical lower electrode in a formation of the dielectric layer; and

forming a second conductive layer on the dielectric layer as an upper electrode.

25. (Previously Presented) The method of Claim 24, wherein the first conductive layer comprises an amorphous silicon layer, a polycrystalline silicon layer and/or a composite layer thereof.

26. (Previously Presented) The method of Claim 24, wherein the reaction-preventing layer is formed by a plasma nitration process at the first temperature below about 600°C, by a chemical vapor deposition process at the first temperature below about 600°C or by an atomic layer deposition process at the first temperature below about 600°C.

27. (Previously Presented) The method of Claim 24, wherein the dielectric layer comprises at least one selected from the group consisting of a TiO_2 layer, an Al_2O_3 layer, an Y_2O_3 layer, a ZrO_2 layer, an HfO_2 layer, a $BaTiO_3$ layer, an $SrTiO_3$ layer and a composite layer thereof.

28. (Previously Presented) The method of Claim 24, wherein the dielectric layer is formed by a chemical vapor deposition process at the second temperature below about 600°C

or by an atomic layer deposition process at the second temperature below about 600°C.

29. (Previously Presented) The method of Claim 24, wherein the second conductive layer comprises one of an amorphous silicon layer, a polycrystalline silicon layer, an Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and/or a composite layer thereof.

30. (Previously Presented) The method of Claim 24, wherein the lower structure comprises a contact plug connected to the cylindrical lower electrode.

31. (Previously Presented) The method of Claim 1, wherein the nitride protection layer comprises an electrically non-conductive layer.

32. (Previously Presented) A method of forming a capacitor on an integrated circuit comprising:

forming a lower electrode on an integrated circuit substrate;

forming an electrically non-conductive protection layer on the lower electrode at a first temperature without a phase change of the lower electrode and without an increase of a resistance of the first lower electrode;

forming a dielectric layer on the electrically non-conductive protection layer at a second temperature substantially the same as the first temperature, wherein the electrically non-conductive protection layer is configured to prevent an oxidation of the lower electrode in a formation of the dielectric layer; and

forming an upper electrode on the dielectric layer.

33. (Previously Presented) A method of forming a capacitor on an integrated circuit comprising:

forming a lower electrode on an integrated circuit substrate;

forming a nitride protection layer on the lower electrode at a first temperature without

a phase change of the lower electrode and without an increase of a resistance of the lower electrode;

forming a dielectric layer on the nitride protection layer at a second temperature substantially the same as the first temperature, wherein the nitride protection layer is configured to prevent an oxidation of the lower electrode in a formation of the dielectric layer; and

forming an upper electrode on the dielectric layer.